FIG. 1

RA0/AN0/OPA+ → 1 20 ↔ RB3/AN7/OPA
RA1/AN1/OPA- → 2 19 ↔ RB2/AN6
RA4/T0CKI ↔ 3 18 ↔ RA7/OSC1/CLKIN/T1CKI
RA5/$\overline{MCLR}$/VPP → 4 17 ↔ RA6/OSC2/CLKOUT
Vss → 5 16 ← VDD
AVss → 6 15 ← AVDD
RA2/AN2/VREF2 ↔ 7 14 ↔ RB7/C2/PSMC1B/$\overline{T1G}$
RA3/AN3/VREF1 ↔ 8 13 ↔ RB6/C1/PSMC1A
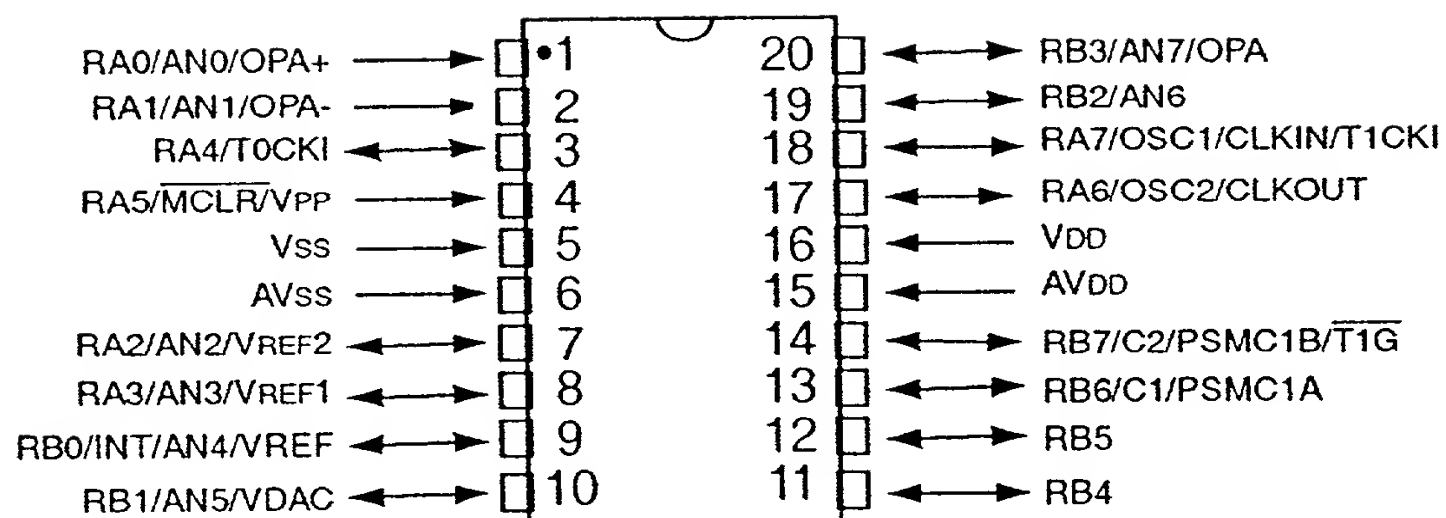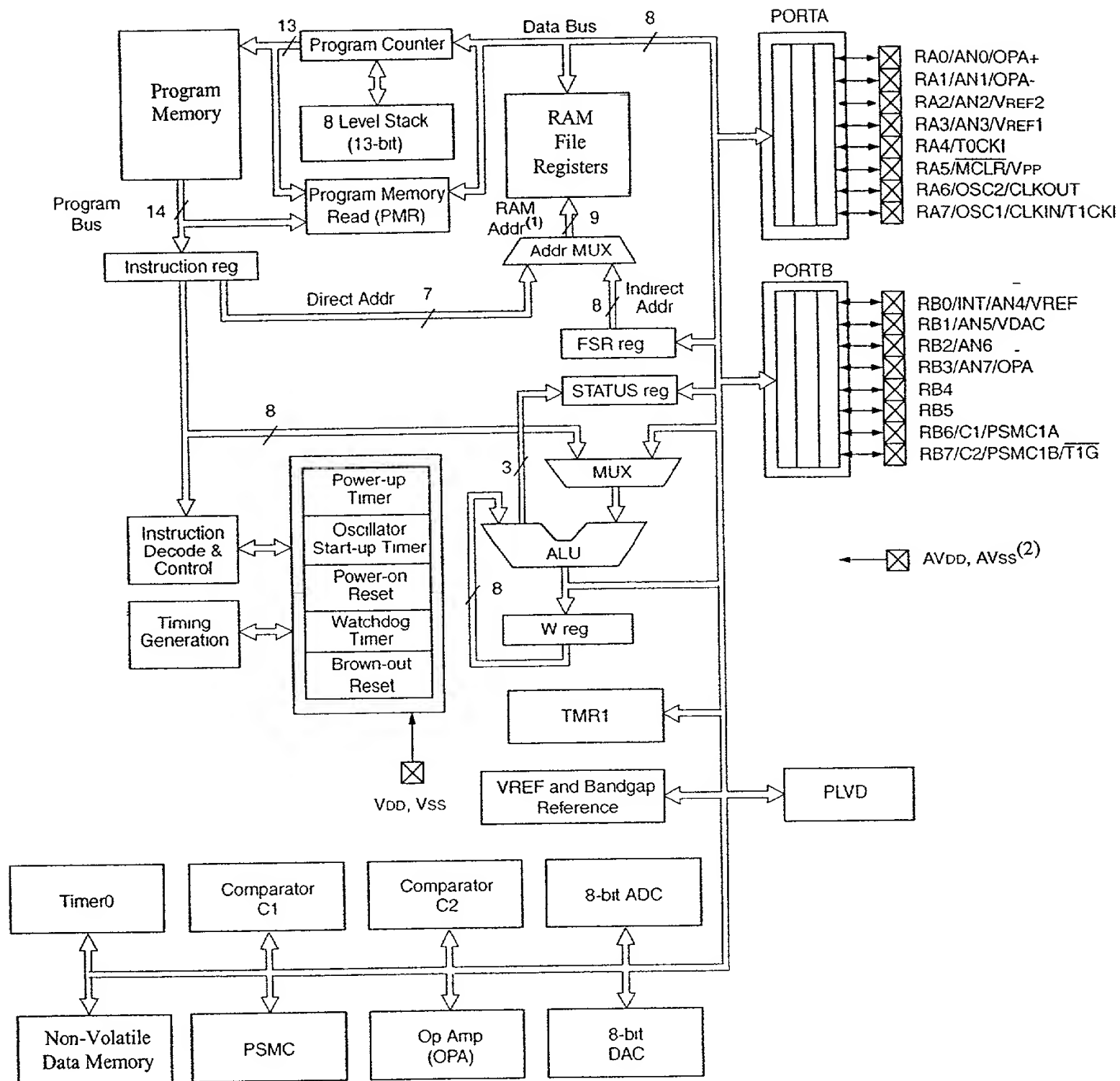RB0/INT/AN4/VREF ↔ 9 12 ↔ RB5
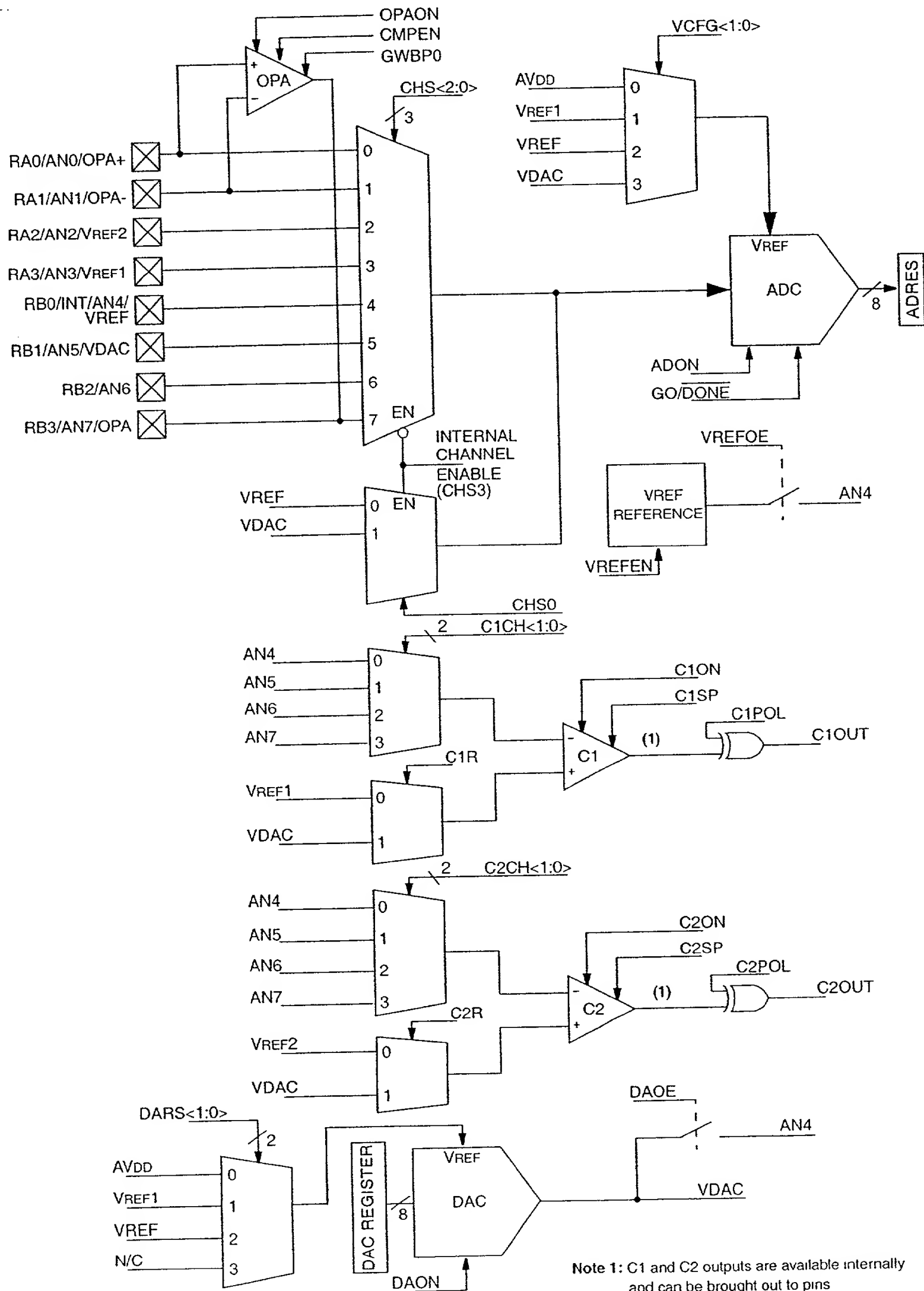RB1/AN5/VDAC ↔ 10 11 ↔ RB4

FIG. 2

FIG. 3

Note 1: Higher order bits are from the STATUS register.

2. AVDD and AVSS pins are used for the following modules: C1, C2, OPA, DAC, ADC, and VREF.

FIG. 4

Legend: C1 = Comparator 1, C2 = Comparator 2, OPA = Operational Amplifier, VREF = Voltage Reference Low.

Note 1: C1 and C2 outputs are available internally and can be brought out to pins